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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,853	03/24/2004	Uday Shah	042390.P18612	8116

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,853	SHAH ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/04, 6/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 3/24/04, 6/8/04, 10/12/04, and 1/10/05 was filed before the mailing date of the non-final rejection on 5/1/06. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The formal drawings filed on 3/24/04 have been approved by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (US 5,880,033) in view of Huang et al. (US 6,242,312).

With respect to Claim 1, Tsai discloses forming a dielectric layer 16 (i.e. silicon dioxide) on a substrate 20. Forming a polysilicon layer 24 having a thickness of about 500 angstroms on the dielectric layer 16. Etching the polysilicon layer 16 to generate a patterned polysilicon layer that has an upper surface and a lower surface (see col. 4 lines 5-53; Figs. 1a and 1b). Tsai discloses that the polysilicon layer has a sidewall that tapers at 88° or 89° with the surface of the substrate 20 (see col. 8 lines 8-22). Tsai fails explicitly disclose the upper surface having a first width that is less than or equal to about 45 angstroms and the lower surface having a second width that is less than or equal to about 40 angstroms. However, Huang discloses an upper surface of polysilicon layer in a gate structure having an upper width of .45 micrometers (i.e. 45 angstroms) (see col. 3 lines 5-10). Thus, Tsai and Huang have the same environment of a plasma etching of a polysilicon layer over a substrate to form a polysilicon gate structure. In a plasma etching environment the etch rate of the wet etch bath can be modified along with the duration of the etching process which will determine the width of the gate electrode. This would result in the width of the gate electrode varying depending upon the desired result. Therefore, one skilled in the art would readily recognize from the combination of Tsai and Huang would result a first width that is less than or equal to about 45 angstroms and the lower surface having a second width that

is less than or equal to about 40 angstroms, wherein the first width is at least about 5 angstroms greater than the second width, since the variation in the first and second widths (i.e. more than 5 angstroms) would shorten the channel length that would increase operation speed of transistor.

With respect to Claim 2, Tsai discloses placing the substrate, after it is covered with the dielectric layer and the polysilicon layer, on a chuck that is positioned within a high density plasma etch tool prior to etching the polysilicon layer (see col. 4 lines 21-65; Figs. 1a, 1b, and 2).

With respect to Claim 3, Tsai discloses wherein the dielectric layer is electrically charged when the polysilicon layer is etched based on the RF current applied to the substrate during the etching process which is in contact with the polysilicon layer (see col. 3 lines 8-20 and col. 6 lines 5-67; Fig. 2).

With respect to Claim 4, Tsai discloses wherein the dielectric layer comprises a material electric layer that is selected from the group consisting of silicon dioxide and a nitrided silicon dioxide and is sufficiently thick to maintain an electric charge for substantially the entire time that the polysilicon layer is etched, the polysilicon layer is between about 100 and about 2,000 angstroms thick, and the polysilicon layer is etched by exposing the polysilicon layer to a plasma derived from chlorine, hydrogen bromide, oxygen, and argon (see col. 3 lines 7-20, col. 4 lines 15-20, and col. 6 lines 5-67).

With respect to Claim 5, Tsai discloses wherein RF bias power of less than about 100 polysilicon layer prior to etching the polysilicon layer (see col. 5 lines 11-25).

With respect to Claim 6, Tsai discloses forming a masking layer on the polysilicon layer prior to etching the polysilicon layer (see col. 4 lines 20-36).

5. Claims 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (US 5,880,033) and Huang et al. (US 6,242,312) as applied to claim 1 above, and further in view of Hobbs et al. (US 6,171,910).

With respect to Claims 7 and 9, Tsai discloses wherein the masking layer is created in part by forming a metal silicide having a thickness of about 500 angstrom (see col. 4 lines 10-35). Tsai-Huang discloses the claimed invention except for explicitly disclose wherein a silicon nitride layer that is between about 100 angstroms and about 500 angstroms thick on the polysilicon layer, then etching the silicon nitride layer by exposing that layer to a plasma to create a hard mask. However, Hobbs discloses forming a silicon nitride layer 166 that is between about 100 angstroms and about 500 angstroms thick on the polysilicon layer 164, then etching the silicon nitride layer 166 by exposing that layer to a plasma to create a hard mask (see 3 lines 20-45 and col. 4 lines 23-60; Figs. 2 and 3). Thus, Tsai-Huang and Hobbs have substantially the same environment of a polysilicon gate etched in a plasma atmosphere. Therefore, one skilled in the art at the time of the invention would readily recognize incorporating a silicon nitride layer for the metal silicide layer of Tsai-Huang, since the silicon nitride layer would provide reliable reflective material during the etching process of the polysilicon layer as taught by Hobbs.

With respect to Claim 8, Hobbs discloses wherein the dielectric layer is a high-k dielectric (see col. 4 lines 18-22 and col. 7 lines 40-46).

With respect to Claims 10-13, Hobbs discloses etching the silicon dioxide layer after the polysilicon layer is etched to generate a patterned silicon dioxide layer. Depositing a second silicon nitride layer on the substrate, the hard mask, and the patterned polysilicon layer. Removing the second silicon nitride layer from part of the substrate to form first and second spacers on opposite sides of the patterned polysilicon layer. Removing the hard mask, the patterned polysilicon layer, and the patterned silicon dioxide layer to generate a trench that is positioned between the first and second spacers. Forming a high-k gate dielectric layer (i.e. titanium oxide) on the substrate at the bottom of the trench and filling at least part of the trench with a metal layer (i.e. tantalum or palladium) that is formed on the high-k gate dielectric layer. Tantalum would have a work function between 3.9eV and about 4.2eV and palladium would have a work function between 4.9 eV and about 5.2eV based on the characteristic of the materials (see col. 3 lines 20-67, col. 4 lines 1- 67, col. 5 lines 1-67, col. 7 lines 41-46; Figs. 2-10).

With respect to Claim 14, Hobbs discloses forming a forming a dielectric layer on the hard mask and the substrate after forming the first and second spacers. Applying a chemical mechanical polishing process to remove the dielectric layer from the hard mask prior to removing the hard mask, the patterned polysilicon layer, and the patterned silicon dioxide layer to generate the trench. Filling only part of the trench with a work function metal 62 that is between about 50 and about 1,000 angstroms thick (i.e. 10 nanometers = 100 angstrom. Forming on the work function metal a trench fill metal

that is selected from the group consisting of tungsten, aluminum. titanium, and titanium nitride (see col. 4 lines 60- 67 and col. 5 lines 1-11).

6. Claims 15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (US 6,171,910) in view of Gardner et al. (US 6,255,698) and Tsai (US 5,880,033).

With respect to Claim 15 and 17-19, Hobbs teaches forming a nitrided silicon dioxide layer 162 on a substrate 10. Forming on the nitrided silicon dioxide layer 162 a polysilicon layer 164 that is between about 100 and about 2,000 angstroms thick. Forming a first silicon nitride layer 166 that is between about 100 and about 500 angstroms thick on the polysilicon layer 164. Etching the first silicon nitride layer 166 , the polysilicon layer 164, and the nitrided silicon dioxide layer 162, to form a hard mask, a patterned polysilicon layer 164, and a patterned nitrided silicon dioxide layer 162. A second layer 24 is deposited on the substrate, the hard mask, and on opposite sides of the patterned polysilicon layer 164. The second layer 24 is removed from part of the substrate 10 and from the hard mask 166 to form first and second spacers on opposite sides of the patterned polysilicon layer 164 by conventional techniques. Forming a dielectric layer 44 on the hard mask and on the substrate 10. Hobbs does not explicitly disclose the material for the side walls made of silicon nitride. However, it is well known in the semiconductor industry to utilize silicon nitride for the material for side walls of a gate structure as evident by Gardner (see col. 11 lines 40-44). Therefore, it would have been obvious to incorporate a material made of silicon nitride for the side walls of Hobbs, since the silicon nitride provides a reliable material for isolation of the gate

electrode as taught by Gardner. Hobbs discloses removing the dielectric layer 44 from the hard mask 166. Removing the hard mask 166, the patterned polysilicon layer 164, and the patterned nitrided silicon dioxide layer 162 to generate a trench 66 that is positioned between first and second spacers 24. Forming a high-k gate dielectric layer 62 (i.e. titanium oxide) on the substrate 10 at the bottom of the trench 66. Filling at least part of the trench with a metal layer 64 (i.e. tantalum or palladium) that is formed on the high-k gate dielectric layer 62. Tantalum would have a work function between 3.9eV and about 4.2eV and palladium would have a work function between 4.9 eV and about 5.2eV based on the characteristic of the materials (see col. (see col. 3 lines 20-67, col. 4 lines 1- 67, col. 5 lines 1-67, col. 7 lines 41-46; Figs. 2-10). Hobbs fails to explicitly disclose wherein the nitrided silicon dioxide layer maintains an electric charge for substantially the entire time that the polysilicon layer is etched. However, Tsai disclose wherein the silicon dioxide layer 26 maintains an electric charge for substantially the entire time that the polysilicon layer is etched based on the RF current applied to the substrate during the etching process which is in contact with the silicon dioxide layer (see col. 3 lines 8-20 and col. 6 lines 5-67; Fig. 2). Thus, Hobbs-Gardner and Tsai have substantially the same environment of a polysilicon gate structure etched in an plasma atmosphere. Therefore, one skilled in the art at the time of the invention would readily recognize having a nitrided silicon dioxide layer maintaining an electric charge during the process of Hobbs-Gardner, since a charge that is applied to the substrate in contact with the silicon dioxide layer would aid in the etching of the polysilicon as taught by Tsai.

With respect to Claim 20, Hobbs discloses forming a forming a dielectric layer on the hard mask and the substrate after forming the first and second spacers. Applying a chemical mechanical polishing process to remove the dielectric layer from the hard mask prior to removing the hard mask, the patterned polysilicon layer, and the patterned silicon dioxide layer to generate the trench. Filling only part of the trench with a work function metal 62 that is between about 50 and about 1,000 angstroms thick (i.e. 10 nanometers = 100 angstrom. Forming on the work function metal a trench fill metal that is selected from the group consisting of tungsten, aluminum. titanium, and titanium nitride (see col. 4 lines 60- 67 and col. 5 lines 1-11).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (US 6,171,910), Gardner et al. (US 6,255,698), and Tsai (US 5,880,033) as applied to claim 15 above, and further in view of Huang et al. (US 6,242,312.

With respect to Claim 16, Hobbs-Gardner-Tsai all fail explicitly disclose the upper surface having a first width that is less than or equal to about 45 angstroms and the lower surface having a second width that is less than or equal to about 40 angstroms. However, Huang discloses an upper surface of polysilicon layer in a gate structure having an upper width of .45 micrometers (i.e. 45 angstroms) (see col. 3 lines 5-10). Thus, Hobbs-Gardner-Tsai and Huang have the same environment of a plasma etching of a polysilicon layer over a substrate to form a polysilicon gate structure. In a plasma etching environment the etch rate of the wet etch bath can be modified along with the duration of the etching process which will determine the width of the gate electrode. This would result in the width of the gate electrode varying depending upon the desired

result. Therefore, one skilled in the art would readily recognize from the combination of Hobbs-Gardner-Tsai and Huang would result a first width that is less than or equal to about 45 angstroms and the lower surface having a second width that is less than or equal to about 40 angstroms, wherein the first width is at least about 5 angstroms greater than the second width, since the variation in the first and second widths (i.e. more than 5 angstroms) would shorten the channel length that would increase operation speed of transistor.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 15-20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 15 of copending Application No. 10/739,173. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application and application

10/739,173 both recite first and second nitrided silicon dioxide layer with a polysilicon layer.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

15. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/May 1, 2006